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**REMARKS**

This paper is responsive to any paper(s) indicated above, and is responsive in any other manner indicated below.

**PENDING CLAIMS**

Claims 1-20 were pending, under consideration and subjected to examination in the Office Action. Appropriate claims have been amended, canceled and/or added (without prejudice or disclaimer) in order to adjust a clarity and/or focus of Applicant's claimed invention. That is, such changes are unrelated to any prior art or scope adjustment and are simply refocused claims in which Applicant is present interested. At entry of this paper, Claims 1, 4-13 and 21 will be pending for further consideration and examination in the application.

**ALL REJECTIONS UNDER 35 USC '102 AND '103 - TRAVERSED**

All 35 USC rejections (i.e., the 35 USC '102 rejection and the 35 USC '103 rejection) are respectfully traversed. However, such rejections have been rendered obsolete by the present clarifying amendments to Applicant's claims, and accordingly, traversal arguments are not appropriate at this time. However, Applicant respectfully submits the following to preclude renewal of any such rejections against Applicant's clarified claims.

All descriptions of Applicant's disclosed and claimed invention, and all descriptions and rebuttal arguments regarding the applied prior art, as previously submitted by Applicant in any form, are repeated and incorporated hereat by reference. Further, all Office Action statements regarding the prior art rejections are

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respectfully traversed. As additional arguments, Applicant respectfully submits the following.

In order to properly support a '102 anticipatory-type rejection, any applied art reference must disclose each and every limitation of any rejected claim. The applied art does not adequately support a '102 anticipatory-type rejection because, at minimum, such applied art does not disclose (or suggest) the following discussed limitations of Applicant's claims.

Applicant's disclosed and claimed invention is directed toward modular computer system arrangements which allow differing kinds of I/O modules to be easily connected to the system without special handling by a user, and which system is not constrained to a specific bus scheme (i.e., differing types of bus schemes can be used). Applicant's disclosed and claimed invention has several novel and distinguishing features which allow achievement of the above objective.

More particularly, as Applicant's arrangements poll I/O modules coupled to its processing unit, the arrangement receives identification information back from each I/O module. That is, each of the I/O modules coupled to Applicant's processing unit may be a differing type of I/O module utilizing different types of bus configurations and device drivers. Applicant's arrangements utilizes the identification information to access a look-up database within memory (see Applicant's FIG. 6, for example), to determine which bus configuration and device drivers should be used (e.g., an a generic configurable bus) should be used for each respective I/O module, and then varies its bus configuration and bus drivers for accessing the differing I/O modules.

In terms of distinguishing language, independent claim 1 and 21, for example, recite the features/limitations: "wherein in accordance with the association of the I/O

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modules with the identification information, said processing module selects from differing preset bus configuration parameters and device drivers, from a memory, for accessing differing types of the I/O modules."

Regarding rebuttal of the previously-applied art, Kiremidjian's arrangement appears to be directed to an arrangement which utilizes a consistent (i.e., unchangeable) bus configuration, and accordingly, Kiremidjian would not have disclosed or suggested the above-mentioned ones of Applicant's features/limitations. None of the other applied art or art of record (alone or in combination with Kiremidjian) cures such major deficiency with respect to such primary reference.

As a second important feature, Applicant's invention may use simplistic arrangements to activate each I/O module sequentially (e.g., from closest to farthest, relative to being connected to a processing module). For example, assume that under Applicant's arrangements, each I/O module stacks onto a previously-installed I/O module using a connector (i.e., each I/O module has an input connector, and an output connector). Further, assume that each I/O module is configured to watch for an activating signal on a line/connector-terminal. If an arrangement utilizes a 16-line connector arrangement, then the arrangement may use each distinct line to poll a different I/O module.

In order to avoid the expense/trouble of having I/O modules each customized to look at a differing one of the 16-lines, Applicant's arrangement requires each I/O module to look at the same predetermined line/connector-terminal (e.g., terminal #1), and utilizes a unique and novel shifting approach to rotate the lines to differing connector terminals upon each module-to-module transition. That is, as illustrated

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by Applicant's FIG. 2, for example, and explained by Applicant's specification text beginning at page 12, line 23, line 1 is connected to terminal 1 of the input connector of the first I/O module layer, but then a predetermined wiring shifting occurs such that line 2 is connected to terminal 1 of the input connector of the second I/O module layer. Such line shifting occurs module-to-module, such that all the lines can be shifted to terminal 1 at one of the layers.

Such arrangement is advantageous because all I/O modules can be configured to look at terminal 1, and a simple (inexpensive) wire shifting method can be used to apply differing lines to differing I/O module layers.

In terms of distinguishing claim language, independent claim 4, for example, recites: "a module exclusive selection part for determining whether an selecting module select signal of module select signals input from a processing module side Input connector is a signal on a predetermined connector terminal position of the input connector, that selects the I/O module, outputting an activate signal when the module select signal is the signal on the predetermined connector terminal position that selects the I/O module, and shifting the module select signals to differing terminals of an output connector in a predetermined shifting when the module select signal input from the input connector is a signal that selects another I/O module;"

Regarding rebuttal of the previously-applied art, Kiremidjian's arrangement appears to pass its "reset" and "xpin/xpout" through its modules, but appears to always keep the same on the same terminals from module-to-module. None of the other applied art or art of record (alone or in combination with Kiremidjian) cures such major deficiency with respect to such primary reference.

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In addition to the foregoing, the following additional remarks from Applicant's foreign representative are also submitted in support of traversal of the rejection and patentability of Applicant's claims.

Regarding claim 10 (now part of clarified independent claim 4), the Examiner asserts that this invention is disclosed in "serial interconnection" in lines 53. to 59, column 2 in the cited Kiremidjian. However, the Examiner's point respectfully appears to represent a miscomprehension.

More particularly, the data outputted by serial signal, which is intended in claim 4 in Applicant's application, is discriminating information (corresponds to ID output signal 150 in, for example, the fourth embodiment of this specification). However, the meaning of "serial interconnection" disclosed in Kiremidjian is that the RESET and POLL control signals are serially connected, and is different from "identification information as a serial signal" of Applicant's invention.

As rebuttal concerning other claims, the problem to be solved aimed in claims 3, 13 (now part of independent claims 1 and 21, respectively) is "providing method for identifying device of I/O module installed without limiting to a specific bus method". For solving this problem, Applicant's arrangement is structured to obtain a parameter of a system bus to be used for a respective module, by using the ID information as the key, before read/write data in bus. That is, for accessing circuit apparatus 510 by a bus, it is necessary to determine the timing parameter of bus control signal. In Applicant's invention, as defined in claims 1 and 21, in accordance with I/O module identified by identifying information input portion and in parallel with the identification information, predetermined bus control parameter and device driver of I/O module are read out of memory, for a respective I/O module. By this structure

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of Applicant's invention, even if the circuit apparatus is of any kind of bus timing parameter, it can be recognized before accessing and it becomes easier for executing access.

While, in all the cited references, timing parameter of bus is known in before hand (for example, it is structurally determined such as connected by ISA bus), and it is structured that all the circuit apparatus can be accessed by the same timing parameter, or condition. Accordingly in Kiremidjian, it becomes possible to access to XIORD signal from right after resetting.

As mentioned in above, the problems to be solved by this invention is not disclosed in any of the cited references, nor is there any way disclosed for solving such problems. Further, the unique structure of Applicant's invention is not disclosed in the cited references.

As a result of all of the foregoing, it is respectfully submitted that the applied art would not support a '102 anticipatory-type rejection or '103 obviousness-type rejection of Applicant's claims. Accordingly, reconsideration and withdrawal of such '102 and '103 rejections, and express written allowance of all of the rejected claims, are respectfully requested.

#### **EXAMINER INVITED TO TELEPHONE**

The Examiner is herein invited to telephone the undersigned attorneys at the local Washington, D.C. area telephone number of 703/312-6600 for discussing any Examiner's Amendments or other suggested actions for accelerating prosecution and moving the present application to allowance.

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### **RESERVATION OF RIGHTS**

It is respectfully submitted that any and all claim amendments and/or cancellations submitted within this paper and throughout prosecution of the present application are without prejudice or disclaimer. That is, any above statements, or any present amendment or cancellation of claims (all made without prejudice or disclaimer), should not be taken as an indication or admission that any objection/rejection was valid, or as a disclaimer of any scope or subject matter. Applicant respectfully reserves all rights to file subsequent related application(s) (including reissue applications) directed to any/all previously claimed limitations/features which have been subsequently amended or cancelled, or to any/all limitations/features not yet claimed, i.e., Applicant continues (indefinitely) to maintain no intention or desire to dedicate or surrender any limitations/features of subject matter of the present application to the public.

### **CONCLUSION**

In view of the foregoing amendments and remarks, Applicant respectfully submits that the claims listed above as presently being under consideration in the application are now in condition for allowance.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR '1.136. Authorization is herein given to charge any shortage in the fees, including extension of time fees and excess claim fees, to Deposit Account No. 01-2135 (Case No. 500.43408X00) and please credit any excess fees to such deposit account.

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Based upon all of the foregoing, allowance of all presently-pending claims is  
respectfully requested.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



Paul J. Skwierawski  
Registration No. 32,173

PJS/slk  
(703) 312-6600